SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, SHIGEKATSU HASEGAWA, a citizen of Japan residing at Chofu-Shi, Tokyo, Japan and NAOTO ENDO, a citizen of Japan residing at Chofu-Shi, Tokyo, Japan have invented certain new and useful improvements in

SYNCHRONIZING CIRCUIT

of which the following is a specification:-

TITLE OF THE INVENTION

SYNCHRONIZING CIRCUIT

BACKGROUND OF THE INVENTION

5   1.   Field of the Invention

The present invention relates to a synchronizing circuit which renders a synchronization between externally provided codes and internal codes.

10   2.   Description of the Related Art

FIG. 1 shows a block configuration of one exmaple of a GPS receiving apparatus in the related art.

The GPS receiving apparatus 1 shown in the figure includes a receiving antenna 3, a receiving unit 4,
15   an information processing device 5 and a display device 5.

The receiving antenna 2 receives GPS signals from GPS satellites 2-1 through 2-n. The GPS signals are signals of 1575.42 MHz. The GPS signals received by the receiving antenna 2 are provided to the receiving unit 4.

20   The receiving unit 4 extracts C/A codes (pseudo-random codes) from the GPS signals, and outputs data according to time difference between different C/A codes. The data output from the receiving unit 4 is provided to the information processing device 5.

25   The information processing device 5, according to the output data of the receiving unit 4, obtains information of latitude, longitude, altitude, time and so forth. The information processing device 5, accordintg to the thus-obtained information, drives the display device 6.
30   The display device 6 displays the information of latitude, longitude, altitude, time and so forth obtained by the information processing device 4.

The receiving unit 4 will now be described.

FIG. 2 shows a block configuration of the receiving unit 4 shown in FIG. 1.

The receiving unit 4 includes a radio-frequency circuit 11, a receiving circuit 12, a CPU 13 and a RAM 14.

5   A received signal is provided to the radio-frequency circuit 11 from the antenna 3. The radio-frequency circuit 11 renders frequency conversion on the thus-provided received signal into a signal in a predetermined frequency band.

10   FIG. 3 shows a block configuration of the radio-frequency circuit 11.

The radio-frequency circuit 11 includes frequency converting parts 21 and 22, and an oscillating circuit 23. An oscillation signal of 18.414 MHz is

15   provided to the oscillating circuit 23 from the receiving circuit 12. The oscillating circuit 23 includes a PLL (Phase Locked Loop) circuit, generates an oscillation signal of 1555.983 MHz from the thus-provided oscillation signal of 18.414 MHz, and provides the thus-generated

20   signal to the frequency converting part 21.

The received signal having a carrier frequency of 1575.42 MHz is provided to the frequency converting circuit 21 from the antenna 3, and also, the oscillation signal of 1555.983 MHz is provided to the frequency

25   converting circuit 21 from the oscillating circuit 23. The frequency converting part 21 multiplies the received signal with the oscillation signal of 1555.983 MHz, and converts the carrier frequency of the received signal into 19.437 MHz.

30   The received signal having thus undergone the frequency conversion by the frequency converting circuit 21 is provided to the frequency converting circuit 22. The oscillation signal of 18.414 MHz is provided to the

frequency converting circuit 22 from the receiving circuit
12. The frequency converting circuit 22 multiplies the
received signal from the frequency converting circuit 21
with the oscillation signal from the receiving circuit 12,
5   and converts the received signal into a signal having a
carrier frequency of 1.023 MHz. The signal obtained
through the conversion by the frequency converting circuit
22 is provided to the receiving circuit 12.

The receiving circuit 12 extracts a satellite
10 code according to the signal provided from the radio-
frequency circuit 11.

FIG. 4 shows a block configuration of the
receiving circuit 12.

The receiving circuit 12 includes a C/A-code
15 generating circuit 31, multipliers 32 through 37, an
oscillating circuit 38, a first detecting circuit 39, a
second detecting circuit 40, a third detecting circuit 41
and a fourth detecting circuit 42.

The signal from the radio-frequency circuit 11
20 is provided to the multipliers 32 and 33. The multipliers
32 and 33 are connected to the oscillating circuit 38.
The oscillating circuit 38 provides an oscillation signal
accordintg to a carrier frequency of an I-signal to the
multiplier 32, and provides an oscillation signal
25 accordintg to a carrier frequency of a Q-signal to the
multiplier 33. The phase of the oscillating circuit 38 is
controlled by a control signal from the CPU 13.

The C/A-code generating circuit 31 generates 3
types of C/A codes in timing according to the control
30 signal from the CPU 13. The three types of C/A codes are
a 0-chip delayed C/A code without delay, a -1/2-chip
delayed C/A code having a delay of -1/2 chip from the 0-
chip delayed C/A code, and a +1/2-chip delayed C/A code

having a delay of +1/2 chip from the 0-chip delayed C/A code. The term 'chip' is a special term in the GPS technical field, and means a unit of a signal when the signal is divided in time axis.

5   The multiplier 32 multiplies the signal from the radio-frequency circuit 11 with the occultation signal from the oscillating circuit 38, and extracts the I-signal. The multiplier 33 multiplies the signal from the radio-frequency circuit 11 with the occultation signal from the

10   oscillating circuit 38, and extracts the Q-signal.

The I-signal extracted by the multiplier 32 is provided to the multipliers 34 through 36. The I-signal is provided to the multiplier 34 from the multiplier 32, and, also, the -1/2-chip delayed C/A code is provided to

15   the multiplier 34 from the C/A-code generating circuit 31. The multiplier 34 multiples the I-signal with the -1/2-chip delayed C/A code.

The I-signal is provided to the multiplier 35 from the multiplier 32, and, also, the 0-chip delayed C/A

20   code is provided to the multiplier 35 from the C/A-code generating circuit 31. The multiplier 35 multiples the I-signal with the 0-chip delayed C/A code.

The I-signal is provided to the multiplier 36 from the multiplier 32, and, also, the +1/2-chip delayed

25   C/A code is provided to the multiplier 36 from the C/A-code generating circuit 31. The multiplier 36 multiples the I-signal with the +1/2-chip delayed C/A code.

The Q-signal is provided to the multiplier 37 from the multiplier 33, and, also, the 0-chip delayed C/A

30   code is provided to the multiplier 37 from the C/A-code generating circuit 31. The multiplier 37 multiples the Q-signal with the 0-chip delayed C/A code.

The multiplication result of the multiplier 34

is provided to the first detecting circuit 39. The multiplication result of the multiplier 35 is provided to the second detecting circuit 40. The multiplication result of the multiplier 36 is provided to the third

5   detecting circuit 41. The multiplication result of the multiplier 37 is provided to the fourth detecting circuit 42.

The first detecting circuit 39 counts, from the multiplication result of the multiplier 34, chips in

10   disagreement between the -1/2-chip delayed C/A code and I-signal, and, outputs the thus-obtained count value C1. The second detecting circuit 40 counts, from the multiplication result of the multiplier 35, chips in disagreement between the 0-chip delayed C/A code and I-

15   signal, and, outputs the thus-obtained count value C2. The third detecting circuit 41 counts, from the multiplication result of the multiplier 36, chips in disagreement between the +1/2-chip delayed C/A code and I-signal, and, outputs the thus-obtained count value C3.

20   The fourth detecting circuit 42 counts, from the multiplication result of the multiplier 37, chips in disagreement between the 0-chip delayed C/A code and Q-signal, and, outputs the thus-obtained count value C4.

The count values C1, C2, C3 and C4 output from

25   the first through fourth detecting circuits 39 through 42 are provided to the CPU 13.

The CPU 13 obtains correlation values b1 through b4 from the count values C1 through C4. The correlation value b1 is a correlation value between the I-signal and -

30   1/2-chip delayed C/A code. The correlation value b2 is a correlation value between the I-signal and 0-chip delayed C/A code. The correlation value b3 is a correlation value between the I-signal and +1/2-chip delayed C/A code. The

correlation value b4 is a correlation value between the Q-signal and 0-chip delayed C/A code.

The correlation values b1 through b4 are obtained by the following formulas assuming that the count

5   value in a case where there is no correlation is 'a':

$$b1 = C1 - a \qquad \cdots \quad (1)$$

$$b2 = C2 - a \qquad \cdots \quad (2)$$

10

$$b3 = C3 - a \qquad \cdots \quad (3)$$

$$b4 = C4 - a \qquad \cdots \quad (4)$$

15   The CPU 13 obtains a correlation d0 between the I-signal and Q-signal, and the internally generated code from the correlation value b2 and correlation b4 by the following formula (5):

20    $$d0 = (b2^2 + b4^2) \qquad \cdots \quad (5)$$

The CPU 13 compares the correlation d0 with a threshold. When the correlation d0 is smaller than the threshold (this means that the correlation between the

25   received signal and internally generated code is small) and also the phase shift amount has reached 1023 chips (a condition in which it is determined that the frequency difference is so large that the predetermined correlation cannot be obtained therebetween although the phase is

30   shifted through the maximum range), the CPU 13 provides a frequency control signal to the oscillating circuit 38. The oscillating circuit 38 controls the frequency of the oscillation signal provided to the multipliers 32 and 33

accordintg to the frequency control signal from the CPU 13. The CPU 13 repeats the above-mentioned operation until the correlation d0 exceeds the threshold (the phase difference therebetween becomes sufficiently small).

5   When the correlation d0 exceeds the threshold, the CPU 13 performs a lock operation. The lock operation is such that CPU 13 controls the oscillating circuit 38 according to the correlation d0, and monitors the correlation between the I-signal and Q-signal, and the

10   internally generated code. The correlation d0 between the I-signal and Q-signal, and the internally generated code is provided to the information processing device 5.

The information processing device 5 renders a synchronization with the signal from the satellite by

15   using the correlation d0 between the I-signal and Q-signal, and the internally generated code provided from the CPU 13, obtains information therefrom, and extracts position information therefrom. A map is displayed by the display device 6, and, a position according to the thus-extracted

20   position information is displayed on the thus-displayed map. Further, the CPU 13 performs the lock operation according to the correlation value b1 and correlation value b3. With regard to the principle and so forth for obtaining position information and so forth from the GPS

25   signal (signal from satellites), they are well known in the GPS technical field, and detailed description thereof is omitted.

However, in such a search method in the related art, only the correlation between one pair of 0-chip delay

30   of I-signal and 0-chip delay of Q-signal is utilized. Accordingly, the C/A-code can be shifted only by one chip every time in the search operation.

Thereby, a considerable time is required for the

search.

SUMMARY OF THE INVENTION

An object of the present invention is to provide
a synchronizing circuit by which it is possible to render
a synchronization at high speed with a simple
configuration.

A synchronizing circuit synchronizing a
predetermined code (0-chip delayed C/A code) with first
and second codes (I-signal and Q-signal) different in
phase, according to the present invention, includes:

a code generating part (31') outputting phase-
shifted code (-1-chip delayed C/A code) shifted in phase
by a predetermined number (-1) of chips from the
predetermined code;

a first correlation detecting part (34, 39)
detecting a correlation between the phase-shifted code (-
1-chip delayed C/A code) from the code generating part
(31') and the first code (I-signal);

a second correlation detecting part (36, 41)
detecting a correlation between the phase-shifted code (-
1-chip delayed C/A code) from the code generating part and
the second code (Q-signal); and

a code shifting part (13) shifting the phase of
the code (0-chip delayed C/A code, -1-chip delayed C/A
code, -1/2-chip delayed C/A code and +1/2-chip delayed C/A
code) generated from the code generating part (31') by a
predetermined number (2) of chips according to the
detection results of the first and second correlation
detecting parts (34, 36, 39, 42).

The first and second codes (I-signal and Q-
signal) may be different in phase by 1/2 chips; and

the code generating part (31') may generate the

phase-shifted code (-1-chip delayed C/A code) shifted in phase by one chip from the predetermined code (0-chip delayed C/A code).

The circuit may further include:

5   a third correlation detecting part (35, 40) detecting a correlation between the predetermined code (0-chip delayed C/A code) and the first code (I-signal); and

a fourth correlation detecting part (37, 42) detecting a correlation between the predetermined code (0-

10   chip delayed C/A code) and the second code (Q-signal).

The code generating part may further generates first and second fraction-shifted codes (-1/2-chip delayed C/A code and +1/2-chip delayed C/A code) shifted from the predetermined code by an interval (1/2 chip) smaller than

15   one chip in opposite directions (plus and minus); and

the circuit further comprises a switch part (101, 102 and 103) switching so that the first correlation detects part (34, 39) detecting a correlation between the first fraction-shifted code (-1/2-chip delayed C/A code)

20   and the first code (I-signal), and the second correlation detecting part (36, 41) detects a correlation between the second fraction-shifted code (+1/2-chip delayed C/A code) and the first code (I-signal).

A GPS receiving apparatus according to the

25   present invention includes:

a receiving unit (4) extracting C/A codes from given GPS signals, and outputting data according to time difference between the different C/A codes; and

an information processing device (5), according

30   to the output data of the receiving unit, obtaining position information,

wherein the receiving unit synchronizes a predetermined code with first and second codes different

in phase derived from each of the GPS signals, comprises:

a code generating part (31') outputting phase-shifted code shifted in phase by a predetermined number of chips from the predetermined code;

5   a first correlation detecting part (34, 39) detecting a correlation between the phase-shifted code from the code generating part and the first code;

a second correlation detecting part (36, 41) detecting a correlation between the phase-shifted code

10   from the code generating part and the second code; and

a code shifting part (13) shifting the phase of the phase-shifted code from the code generating part by a predetermined number of chips according to the detection results of the first and second correlation detecting

15   parts.

Thereby, by detecting the correlation using not only the predetermined code (0-chip delayed C/A code) but also the phase-shifted code (-1-chip delayed C/A code) shifted by an integral number of chips for search

20   operation, it is possible to reduce the number of times of code shifting needed for the search operation. Accordingly, it is possible to render high-speed synchronization of the predetermined code to the given codes (I-signal and Q-signal).

25   Other objects and further features of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings.

30   BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block configuration of one exmaple of a GPS receiving apparatus in the related art;

FIG. 2 shows a block configuration of a

receiving unit shown in FIG. 1;

FIG. 3 shows a block configuration of a radio-frequency circuit shown in FIG. 2;

FIG. 4 shows a block configuration of a

5   receiving circuit shown in FIG. 2;

FIG. 5 shows a block configuration of a receiving circuit in one embodiment of the present invention; and

FIG. 6 shows a flow chart of operation rendered

10   by a CPU in the first embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the present invention will now be described with reference to figures.

15   FIG. 5 shows a block configuration of a receiving circuit (corresponding to the receiving circuit 12 in the related art shown in FIG. 4) of the embodiment of the present invention. In FIG. 5, the same reference numerals are give to the parts/components same as those in

20   FIG. 4, and description thereof is omitted. Further, a GPS receiving apparatus according to the present invention is similar to the GPS receiving apparatus in the related art described above with reference to FIGS. 1 through 3, but the receiving circuit is changed from the receiving

25   circuit 12 described above with reference to FIG. 4 into the receiving circuit 100 which will now be described with reference 5.

The receiving circuit 100 of the embodiment of the present invention is different from the receiving

30   circuit 12 described above by the following points: the C/A codes output from the C/A-code generating circuit 31' (corresponding to the above-described C/A-code generating circuit 31) are four types thereof, and, also, three

switches 101, 102 and 103 are newly provided.

The C/A-code generating circuit 31' generates, in addition to the -1/2-chip delayed C/A code, 0-chip delayed C/A code and +1/2-chip delayed C/A code, -1-chip

5 delayed C/A code delayed from the 0-chip delayed C/A code by one chip.

The -1/2-chip delayed C/A code and -1-chip delayed C/A code are provided to the switch 101 from the C/A-code generating circuit 31'. The switch 101 selects

10 either the -1/2-chip delayed C/A code or -1-chip delayed C/A code according to a switching control signal from the CPU 13, and provides the thus-selected code to the multiplier 34.

The multiplication result of the multiplier 32

15 and the multiplication result of the multiplier 33 are provided to the switch 102. The switch 102 selects either the multiplication result of the multiplier 32 or the multiplication result of the multiplier 33 according to a switching control signal from the CPU 13, and provides the

20 thus-selected one to the multiplier 36.

The +1/2-chip delayed C/A code and -1-chip delayed C/A code are provided to the switch 103 from the C/A-code generating circuit 31'. The switch 103 selects either the +1/2-chip delayed C/A code or -1-chip delayed

25 C/A code according to a switching control signal from the CPU 13, and provides the thus-selected code to the multiplier 36.

Operation of this embodiment of the present invention will now be described.

30 FIG. 6 shows an operation flow chart of the CPU 13 of the embodiment of the present invention.

The CPU 13 executes steps S1 through S8.

In the step S1, the switches 101 through 103 are

switched into states for search operation. In the search operation, the switch 101 is switched so that the -1-chip delayed C/A code from the C/A-code generating circuit 31' is provided to the multiplier 34. Further, the switch 102

5   is switched so that the Q-signal from the multiplier 33 is provided to the multiplier 36. The switch 103 is switched so that the -1-chip delayed C/A code from the C/A-code generating circuit 31' is provided to the multiplier 36.

Then, the step S2 is executed. In the step S2,

10   the count values C1 through C4 are input from the first through fourth detecting circuit 39 through 42 to the CPU 13.

The CPU 13 obtains a correlation d0 and a correlation d10 from the count values C1 through C4 input

15   in the step S2.

The correlation d10 is obtained from the count value C1 from the first detecting circuit 39 and the count value C3 from through third detecting circuit 41.

First, from the count values C1 and C3, the

20   correlation values b1 and b3 are obtained by the above-mentioned formulas (1) and (3). Then, from the correlation values b1 and b3, the correlation d10 is obtained by the following formula (6):

25       $d10 = (b1^2 + b3^2)$ $\cdots$ (6)

The correlation d0 is obtained from the count value C2 from the second detecting circuit 40 and the count value C4 from through fourth detecting circuit 42.

30   First, from the count values C2 and C4, the correlation values b2 and b4 are obtained by the above-mentioned formulas (2) and (4). Then, from the correlation values b2 and b4, the correlation d0 is

obtained by the above-mentioned formula (5).

The correlation d10 corresponds to a correlation between the -1-chip delayed C/A code and the I-signal and a correlation between the -1-chip delayed C/A code and the Q-signal. The correlation d0 corresponds to a correlation between the 0-chip delayed C/A code and the I-signal and a correlation between the 0-chip delayed C/A code and the Q-signal.

After obtaining the correlations d0 and d10 in the step S2, the CPU 13 executes the step S3. In the step S3, the CPU 13 determines whether or not the correlations d0 and d10 are larger than a threshold. When the correlations d0 and d10 are smaller than the threshold, the step S4 is executed.

In the step S4, it is determined whether or not the phase shift amount of the C/A codes output from the C/A-code generating circuit 31' is such that shift has been rendered for 1023 chips equal to all the chips of the C/A code. When it is determined in the step S4 that the chip shift of 1023 chips has been rendered, it can be determined that the multiplication results of the multipliers 32 and 33 have an error. Accordingly, the CPU 13 controls the frequency of the oscillation signal provided to the multipliers 32 and 33 from the oscillating circuit 38. After thus changing the frequency in the step S4, the process is returned to the step S1, and the search operation is performed again.

Further, when the shift amount of the C/A codes has not reached 1023 chips in the step S4, the step S6 is executed. In the step S6, a shift control signal is provided to the C/A-code generating circuit 31', and the C/A codes generated from the C/A-code generating circuit 31' are shifted by 2 chips. After the C/A codes are

shifted in the step S6, the process is returned to the step S2, and the operation is continued.

When the correlations d0 and d10 are equal to or larger than the threshold, it can be determined that the lock (phase lock) operation can be rendered, and, therefore, the step S7 is executed.

In the step S7, the switches 101 through 103 are switched to states for the lock operation.

The switch 101 is switched so that the -1/2-chip delayed C/A code is provided to the multiplier 34 from the C/A-code generating circuit 31'. The switch 102 is switched so that the multiplication result of the multiplier 32 is provided to the multiplier 36. The switch 103 is switched so that the +1/2-chip delayed C/A code from the C/A-code generating circuit 31' is provided to the multiplier 36.

Thereby, the count value C1 output from the first detecting circuit 39 is a correlation value between the I-signal and -1/2-chip delayed C/A code. The count value C2 output from the second detecting circuit 40 is a correlation value between the I-signal and 0-chip delayed C/A code. The count value C3 output from the third detecting circuit 41 is a correlation value between the I-signal and +1/2-chip delayed C/A code. The count value C4 output from the fourth detecting circuit 42 is a correlation value between the Q-signal and 0-chip delayed C/A code.

After the switches 101 through 103 are thus switched into the states for the lock operation, the lock operation is performed in the step S8.

In the lock operation, the CPU 13 obtains the correlation value b2 and b4 from the count value C2 from the second detecting circuit 40 and the count value C4

from the fourth detecting circuit 42 by the formulas (2)
and (4), obtains the correlation d0 by the formula (5),
controls the oscillating circuit 38 so that the
correlation d0 becomes not larger than a threshold, and

5   locks the frequency. At this time, control is rendered
such that the correlation value b4 becomes smaller and the
correlation value b2 becomes larger.

Further, the CPU 13 obtains the correlation
value b1 and b3 from the count value C1 from the first

10   detecting circuit 39 and the count value C3 from the third
detecting circuit 41 by the formulas (1) and (3), obtains
the correlation d10 by the formula (6), controls the C/A-
code generating circuit 31' so that the correlation d10
becomes not larger than a threshold, and locks the phase.

15   At this time, control is rendered such that the difference
between the correlation values b1 and b3 becomes smaller.

According to the present invention, the
correlation between the -1-chip delayed C/A code and the
I-signal and the correlation between the -1-chip delayed

20   C/A code and the Q-signal, and, also, the correlation
between the 0-chip delayed C/A code and the I-signal and
the correlation between the 0-chip delayed C/A code and
the Q-signal are obtained, and are utilized in the search
operation. Thereby, it is possible to render the search

25   for two chips at once. Accordingly, it is possible to
render the search at a speed twice that of the related art,
and to perform the search at high speed.

At this time, the configuration of the C/A-code
generating circuit 31' needs to output -1-chip delayed C/A

30   code additionally in comparison to the related art.
Accordingly, increase in circuit scale is within a small
amount. Further, by adding the switches 101 through 103,
it is possible to render the lock operation similarly to

that in the related art.

The switches 101 through 103 may be built in the C/A-code generating circuit 31' integrally.

5   The present invention is not limited to the above-described embodiment, and variations and modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese priority application No. 2000-25771, filed on February 2,

10   2000, the entire contents of which are hereby incorporated by reference.